Amendments to the Specification

Please amend paragraph [0061] as follows:

Referring to Figure 3B, supply exceed detector 380 includes a PMOS transistor having its gate terminal coupled to the Vdd voltage, its drain terminal coupled to a current source providing a current [[IDO]] IDC and a source terminal coupled to receive the data pulse voltage. An inverter is coupled to the drain terminal of the PMOS transistor. If the data pulse voltage does not exceed the Vdd voltage by the threshold voltage of the PMOS transistor, the PMOS transistor will be turned off and the voltage at the drain terminal is near the Vss voltage and the LATCHl signal is not asserted. If the data pulse voltage exceeds the Vdd voltage by the threshold voltage of the PMOS transistor, the PMOS transistor will be turned on and the voltage at the drain terminal is pulled up, tripping the inverter output voltage and thereby asserting the LATCH1 signal.